In the Abstract:

The amended Abstract is as follows, as marked up in Appendix A:

A method of making an electronic package. The method includes forming a semiconductor chip and an multi-layered interconnect structure. The semiconductor chip includes a plurality of contact members on one of its surfaces that are connected to the multi-layered interconnect structure by a plurality of solder connections. The formed multi-layered interconnect structure is adapted for electrically interconnecting the semiconductor chip to a circuitized substrate (eg., circuit board) with another plurality of solder connections and includes a thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of the solder connections between said first plurality of electrically conductive members and the semiconductor chip. The method forms the electronic package to further include a dielectric material having an effective modulus to assure sufficient compliancy of the multi-layered interconnect structure during operation.

In the Specification:

The amended paragraph beginning on page 16, line 8 is as follows, as marked up in Appendix A:

The electronic package of the present invention can be assembled to a circuitized substrate 100 having a plurality of contact pads 103 on one of its surfaces. As described, these contact pads can be comprised of copper or aluminum or another suitable metal and can be coated with a layer of solder paste (not shown). The second plurality of solder connections of the